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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. Of: HONDA
Serial No.: 09/712,105
Filed: November 14, 2000
For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD...
Group: 2811
Examiner: THAI, LUAN C. DOCKET: NEC 00USFP553

The Assistant Commissioner of Patents
Washington, D.C. 20231

AMENDMENT B

Dear Sir:

This Amendment is being filed in response to the Official Action mailed March 13, 2002.

Please amend the Application as follows:

IN THE TITLE:

Please amend the Title to read as follows:

--SEMICONDUCTOR DEVICE HAVING IMPROVED RESISTANCE TO THERMAL
AND MECHANICAL STRESS--

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 1, line 13, with the following rewritten paragraph:

--In recent semiconductor devices, new forms of packages have been developed to
comply with demands for electronic devices having high performance, small size, light weight,
and high speed. Smaller and slimmer devices have been realized by high integration of

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semiconductor chips to be mounted, and much higher performance and speed are aimed at electronic devices. A package according to FCBGA (Flip Chip Ball Grid Array) method has appeared.--

Please replace the paragraph bridging pages 3-4, beginning at line 26, with the following rewritten paragraph:

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--A package according to the FCBGA method is generally used for a large-scale semiconductor integrated circuit (LSI) having high performance, and the product itself is expensive. Therefore, if an error is detected in other parts than the semiconductor chip through an electrical selection process after actual installation of the semiconductor chip, the semiconductor chip is detached from the multi-layer printed circuit board and is used again. In the process of the detachment, as shown in Fig. 1C, the non-defective semiconductor chip 31 is heated and suctioned and pulled up by a suction heat tool 33, while the bump connecting sections is melted. Thus, the non-defective semiconductor chip 31 is detached from the multi-layer printed circuit board 32.--

Please replace the paragraph beginning at page 5, line 2, with the following rewritten paragraph:

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--In conjunction with the above description, a chip size package is disclosed in Japanese Laid Open Patent Application (JP-A-Heisei 9-64236). In this reference, a chip 10 is connected to a laminate circuit board 20 via direct through-holes 30 in a flip-chip manner. The laminate circuit board 20 has the same size as the chip 10. A gap between the laminate circuit board 20 and the chip 10 is filled with under-fill (40). The chip 10 is connected to external terminals 50 via wiring lines 21 to 24 and via-holes 31. The whole chip 10 including the board 20 is covered other than openings 61 by encapsulant.--

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Please replace the paragraph bridging pages 6-7, beginning at line 22, with the following rewritten paragraph:

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--Also, a test connector is disclosed in Japanese Patent No. 2,658,831. In this reference, the test connector is produced through an electrode section opening process, an electrode embedding process and an electrode finishing process. A test semiconductor device to be tested has bumps on its surface. The bumps are connected by a flip chip method in which wiring lines are not used. The test connector has a sheet-like shape and electrodes supported by a supporting substrate are connected to the bumps for an electric test. In the electrode opening process, openings for electrode sections are formed in a sheet using a punch and a die. in the electrode section embedding process, electrodes are inserted in the openings and then heat-resistant insulating material is injected and hardened as an insulating film. In the electrode section finishing process, the sheet is removed. Thus, ends of each of the electrodes protrude from the insulating film.--

Please replace the paragraph bridging pages 7-8, beginning at line 26, with the following rewritten paragraph:

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--Still another object of the present invention is to provide a semiconductor device, in which damage during recovery process for peripheral devices including an installation board can be avoided to realize low costs.--

Please replace the paragraph beginning at page 8, line 4, with the following rewritten paragraph:

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--In order to achieve an aspect of the present invention, a semiconductor device includes pads formed on a semiconductor chip, conductive sections connected to the pads, respectively, conductive bumps on surfaces of the conductive sections, and an insulating film covering the

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semiconductor chip other than the surfaces of the conductive sections. The insulating film includes a stress buffering layer in a lateral direction of the conductive sections to relax a stress applied to the bumps.--

Please replace the paragraph beginning at page 9, line 10, with the following rewritten paragraph:

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--Also, the insulating film may comprise a first and a second insulating film and the conductive section may be connected to the pad via a wiring pattern provided on the semiconductor chip through the first insulating film. In this case, it is desirable that the wiring pattern is formed of copper (Cu). Also, the wiring pattern may extend to adjust a pitch between the conductive bump and another conductive bump. Further, the first insulating film may include a passivation film covering the semiconductor chip other than the pads, and a second insulating film formed on the passivation film. In this case, it is desirable that the second insulating film has a pyrolysis temperature of 200° C or more. In addition, the second insulating film may be formed of a photosensitive material.--

Please replace the paragraph beginning at page 14, line 4, with the following rewritten paragraph:

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--Next, as shown in Fig. 2B, an insulative resin film (insulating layer) 20 is formed on the pad electrodes 12 and a passivation film 13. The insulating resin film 20 is made of inorganic material such as SiO₂, or organic material such as polyimide (PI). Resin material having a pyrolysis temperature of 200° C or more is used for the insulating resin film 20. When material of a thermal hardening component is mixed in the insulating resin film 20, heat treatment is carried out at a predetermined temperature thereby to promote bridging reaction of resin components. Thus, predetermined physical and chemical properties are attained.--

IN THE CLAIMS:

Kindly cancel claims 1-24, without prejudice.

Please add new claims 25-49 reading as follows:

- ✓ --25. A semiconductor device, comprising:
- pads formed on a semiconductor chip;
 - conductive sections connected to said pads, respectively;
 - first conductive bumps on surfaces of said conductive sections and covered other than at their top surfaces with a first electrically insulative stress buffering layer; and
 - second conductive bumps on exposed top surfaces of said first conductive bumps, and covered other than at their top surfaces with a second electrically insulating stress buffering layer.
- 49 26. The semiconductor device according to claim 25, wherein said first stress buffering layer has an elastic modulus in a range of 0.01 to 8 Gpa.
27. The semiconductor device according to claim 25, wherein said second stress buffering layer has an elastic modulus in a range of 0.01 to 8 Gpa.
- ✓ 28. The semiconductor device according to claim 25, wherein said first stress buffering layer is formed of material comprising at least one selected from the group consisting of an epoxy-based resin, a silicon-based resin, a polyimide-based resin, a polyolefin-based resin, a cyanate-ester-based resin, a phenol-based resin, a naphthalene-based resin, and a fluorine-based resin.
- ✓ 29. The semiconductor device according to claim 25, wherein said second stress buffering layer is formed of material comprising at least one selected from the group consisting of an epoxy-based resin, a silicon-based resin, a polyimide-based resin, a polyolefin-based resin,

a cyanate-ester-based resin, a phenol-based resin, a naphthalene-based resin, and a fluorine-based resin.

✓ 30. The semiconductor device according to claim 25, wherein said conductive sections are connected to said pad via a wiring pattern provided on said semiconductor chip.

✓ 31. The semiconductor device according to claim 30, wherein said wiring pattern is formed of copper (Cu).

✓ 32. The semiconductor device according to claim 30, wherein said wiring pattern extends to adjust a pitch between said conductive bump and another conductive bump.

✓ 33. The semiconductor device according to claim 25, and further including a passivation film underlying said first stress buffering layer and covering said semiconductor chip other than said pads.

✓ 34. The semiconductor device according to claim 33, and further including a separate insulating film formed between said passivation film and said first stress buffering layer.

35. The semiconductor device according to claim 34, wherein said separate insulating film has a pyrolysis temperature of 200° C or more.

36. The semiconductor device according to claim 34, wherein said separate insulating film is formed of a photosensitive material.

37. A semiconductor device, comprising:
pads formed on a semiconductor chip;
conductive sections connected to said pads, respectively;
conductive columns on surfaces of said conductive sections and covered other than at their top surfaces with an electrically insulating stress buffering layer; and
conductive bumps on exposed surfaces of said conductive columns.

38. The semiconductor device according to claim 37, wherein said stress buffering layer has an elastic modulus in a range of 0.01 to 8 Gpa.

39. The semiconductor device according to claim 37, wherein said stress buffering layer is formed of material comprising at least one selected from the group consisting of an epoxy-based resin, a silicon-based resin, a polyimide-based resin, polyolefin-based resin, a cyanate-ester-based resin, a phenol-based resin, a naphthalene-based resin, and a fluorine-based resin.

40. The semiconductor device according to claim 37, wherein said conductive sections are connected to said pad via a wiring pattern provided on said semiconductor chip.

41. The semiconductor device according to claim 40, wherein said wiring pattern is formed of copper (Cu).

42. The semiconductor device according to claim 40, wherein said wiring pattern extends to adjust a pitch between said conductive columns.

43. The semiconductor device according to claim 40, and further including a passivation underlying said first stress buffering layer and covering said semiconductor chip other than said pads.

44. The semiconductor device according to claim 43, and further including a second insulating film formed between said passivation film and said stress buffering layer.

45. The semiconductor device according to claim 44, wherein said second insulating film has a pyrolysis temperature of 200° C or more.

46. The semiconductor device according to claim 44, wherein said second insulating film is formed of a photosensitive material.

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47. The semiconductor devices according to claim 37, wherein said conductive columns comprise a metal material selected from the group consisting of Cu, Ni, Pb, Sn, Al, Fe and In as a main component.

48. The semiconductor device according to claim 37, wherein said conductive columns have a height of 10 to 200 μm .

49. The semiconductor device according to claim 37, wherein said conductive columns are circular in cross section.--

REMARKS

The Specification has been amended to correct minor clerical errors, and to employ more idiomatic English. No new matter has been entered by any of the foregoing amendments. Pursuant to 37 CFR § 1.121, a marked copy of the amended Specification paragraphs showing changes made therein accompanies this Amendment.

The claims have been rewritten to address the 112 Rejections, the objections to the drawings, and also to better define the claimed invention, and to distinguish the claimed invention from the prior art. More particularly, new independent claim 5 has been directed specifically to the embodiment of Fig. 3, in which first conductive bumps are covered with a first stress buffering layer, and second conductive bumps are formed on the first conductive bumps, and are covered by a second stress buffering layer. And, new independent claim 37 is directed to the embodiment of Fig. 4, in which conductive columns are formed on conductive sections connected to the pads, and the conductive columns are covered by a stress buffering layer. It is submitted that none of the art of record teaches or suggests either claim structure. At best, the primary reference, Chakravorty, teaches a single encapsulant layer formed over a first

plurality of metal bumps, while the secondary references do not even teach a first encapsulant layer. Thus, no combination of any of the art of record reasonably could be said to achieve or render obvious any of the claims. Accordingly, no specific discussion of the art rejections is believed necessary.

Claims 13-24 have been canceled and are being pursued in a Divisional Application. The title has been amended to conform to the patented invention.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

Respectfully submitted,



Norman P. Soloway
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Reg. No. 24,315

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on Nov 1, 2002, at Tucson, Arizona.

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